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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Balaji Prabhakar, et al.	
Serial No.: Not yet assigned	Group: 2662
Filed: concurrently herewith	Examiner: Thien D. Tran
For: "SWITCHING SYSTEMS AND METHODS OF OPERATION OF SWITCHING SYSTEMS"	Our Ref: B-3457DIV 619142-7
	Date: November 13, 2001

Commissioner of Patents and Trademarks
BOX NEW PATENT APPLICATION
Washington, D.C. 20231

Sir:

The above-identified application is a division of U.S. Patent Application Serial No. 09/071,085 filed on May 1, 1998.

Prior to examining this divisional application, please replace the abstract as filed with the amended abstract as enclosed herewith.

It is also respectfully requested that the following amendment be made to the claims.

IN THE CLAIMS

Please add new Claims 16-32 to the above-identified application. A clean copy of Claims 16-32 is presented on the following pages 2-6 of this preliminary amendment.

16. (New) A method as claimed in claim 1, wherein the step of noting the temporal order comprises adding an urgency indicator to the packets arriving at any of the input stages.

17. (New) A method as claimed in claim 16, wherein the method of operation of the switching system further comprises the step of placing each packet in each output stage in a position dependent upon the urgency indicator added to the packet.

18. (New) A system as claimed in claim 12, further comprising a means for adding an urgency indicator to said each received packet based on said temporal order.

19. (New) A system as claimed in claim 18, further comprising means for placing each packet in each output stage in a position dependent upon the urgency indicator added to each received packet.

20. (New) A method of operation of a combined-input-and-output-queued switching system, the switching system comprising:

a plurality of output stages each operable to supply packets of data to a respective output line;

a plurality of input stages each operable to receive packets of data on a respective input line, each received packet being destined for at least a respective one of the output stages; and

a transfer stage operable to transfer packets of data from any of the input stages to those of the output stages for which those packets are destined; and

the method of operation of the switching system comprising the steps of:

for each output stage, adding an urgency indicator to each received packet noting the temporal order in which the packets destined for that output stage are received by the input stages; and

controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stage to that output stage based on said urgency indicator.

21. (New) A method as claimed in claim 20, wherein:

the system operates according to time slots such that:

no more than one packet is received by each input stage during each time slot; and

no more than one packet is supplied by each output stage during each time slot; and

each time slot is divided into a plurality of phases such that:

no more than one packet is transferred from each input stage by the transfer stage during each phase; and no more than one packet is transferred to each output stage by the transfer stage during each phase.

22. (New) A method as claimed in claim 21, wherein the controlling step includes the step, during each phase and for each output stage, of:

selecting that one of the input stages, if any, having that one of the packets which are destined for that output stage which is earliest in the noted temporal order; and

transferring that one packet from the selected input stage to that output stage unless there is input contention due to the selected input stage also having been selected for another of the output stages.

23. (New) A method as claimed in claim 22, wherein the controlling step includes the step, if there is such input contention, of selecting that one of the output stages whose destined packet is earliest in the noted temporal order, unless there is none which is

earliest.

24. (New) A method as claimed in claim 23, wherein the output stages have a predetermined ranking, and wherein the controlling step includes the step, if none of the packets is earliest as aforesaid, of selecting between the output stages in accordance with the predetermined ranking.

25. (New) A method as claimed in claim 20, wherein each input stage comprises a plurality of input buffers, one for each output stage, the method further including the step of placing each received packet in that one of the input buffers for the input line on which that packet is received and for the output stage for which that packet is destined.

26. (New) A method as claimed in claim 20, wherein each output stage comprises a respective output buffer for the packets, and the packets are output from the respective output buffer to the respective output line in dependence upon the noted temporal order of the packets in the respective output buffer.

27. (New) A combined-input-and-output-queued switching system comprising:

a plurality of output stages each operable to supply packets of data to a respective output line;

a plurality of input stages each operable to receive packets of data on a respective input line, each received packet being destined for at least a respective one of the output stages;

a transfer stage operable to transfer packets of data from any of the input stages to those of the output stages for which those packets are destined; and

a scheduling processor for:

(1) adding an urgency indicator to said each received packet based on a temporal order for each output stage, the temporal order being the sequence in which the packets destined for each output stage are received by the input stages; and

(2) controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stages to that output stage based on said urgency indicator.

28. (New) A system as claimed in claim 27, wherein each output stage comprises a respective output buffer for the packets, and the packets are supplied from that buffer to the respective output line in dependence upon the urgency indicator of the packets in the respective output buffer.

29. (New) A system as claimed in claim 27, wherein each input stage comprises an input buffer for each output stage.

30. (New) A NxN combined-input-and-output-queued switching system comprising:

a plurality of output stages each operable to supply packets of data to a respective output line;

a plurality of input stages each operable to receive packets of data on a respective input line, each received packet being destined for at least a respective one of the output stages;

a transfer stage operable to transfer packets of data from any of the input stages to those of the output stages for which those packets are destined;

a temporal order detector for detecting, for each output stage, the temporal order in which the packets destined for that output stage are received by the input stages; and

a scheduling processor for controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stages to that output stage in the detected temporal order.

31. (New) A system as claimed in claim 30, wherein each output stage comprises a respective output buffer for the packets, and the packets are supplied from that buffer to the respective output line in dependence upon the detected temporal order of the packets in the respective output buffer.

32. (New) A system as claimed in claim 30, wherein each input stage comprises an input buffer for each output stage.

REMARKS

The Applicant maintains his position in the response dated March 26, 2001, during prosecution of the parent application, that Cisneros does not disclose, teach or suggest, the following elements as recited by claim 1 of the parent application and the present application:

> "the method of operation of the switching system comprising the steps of:
>
> for each output stage, noting the temporal order in which the packets destined for that output stage are received by the input stages; and
>
> controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stages to that output stage in the noted order."

or the features as recited by claim 12 of the parent application and the present application "means for detecting, for each output stage, the temporal order in which the packets destined for that output stage are received by the input stages; and means for controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stages to that output stage in the detected temporal order."

In the Final Rejection related to the parent application dated May 8, 2001, the Examiner states that "Cisneros discloses a switching system comprising: each output port connected to an input queuing

buffer. In queuing buffer, packets flow in sequence of first in first out order or temporal order (Fig. 5, Col. 7, line 43-45). Controlling the transfer stage for each output stage, so that the packets destined for that output stage are transferred from the input stage to that output stage in queuing order or noted order (Col. 7 line 37-43, Col. 19 line 60-25)". Applicant respectfully disagrees with the Examiner.

Claim 1 of the present application recites "for each output stage, noting the temporal order in which the packets destined for that output stage are received by the input stages". Thus, the temporal order, or the order at which the packets are received at the switch, is noted for each output stage. In addition, claim 1 also recites "controlling the transfer stage so that, for each output stage, the packets destined for that output stage are transferred from the input stages to that output stage in the noted order ". Thus, the transfer of packets from the input stages to a output stage is determined by the order upon which the packets are received at the switch for the given output stage.

Cisneros does not teach or suggest a noting the temporal order in which the packets destined for that output stage are received by the input stages, or controlling the transfer stage so that, for each output stage, the packets are transferred in the noted order. First, Cisneros has a plurality of input modules, each with a FIFO queue, see col. 7, lines 43-44. Thus, the temporal order of the packets arriving at the input stages are kept, but the temporal order of packets arriving at different input stages destined for the same output stage is lost. Consequently, Cisneros teaches noting a temporal order of an individual input stage rather than the output stages. Second, Cisneros teaches transfer from input stages to output stages is based on the address and the accompanying priority

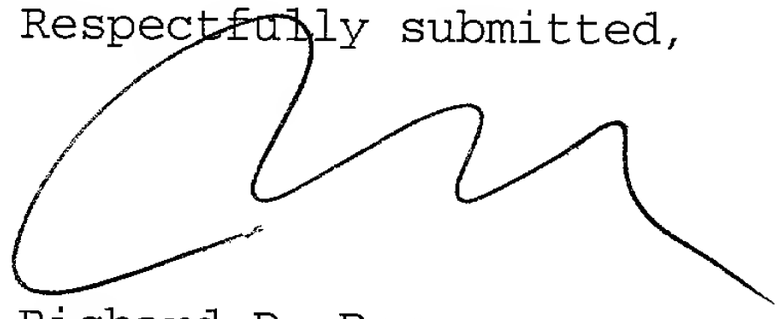
information for the cells situated at the heads of their internal queues (See col. 7, lines 52-60). Priority information is defined as being part of the ATM cell (col. 7, lines 28-29). Thus, the transfer of packets from the input stages to an output stage is determined by the priority information in the ATM cell, and not upon the noted temporal order in which the packets are received at the switch for the given output stage.

Due to the reasons stated above, the Applicant believes that the divisional application is patentable over the cited prior art and is in condition for allowance.

To more describe the unique features of the present application in other ways, the Applicant has added new Claims 16-32. Amendment of the subject application is respectfully requested.

An amended abstract is enclosed. The abstract has been shortened to comply with current U.S.P.T.O. practice.

Respectfully submitted,



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enclosure: Amended Abstract (1 page)

(Amended)

ABSTRACT OF THE DISCLOSURE

Architectures based on a non-blocking fabric, such as a crosspoint switch, are attractive for use in high-speed LAN switches, ATM switches and IP routers. These fabrics, coupled with memory bandwidth limitations, dictate that queues be placed at the input of the switch. But it is well known that input-queueing can lead to low throughput, and does not allow the control of latency through the switch. This is in contrast to output-queueing, which maximizes throughput, and permits the accurate control of packet latency through scheduling. A switch is disclosed with virtual output queueing at the input and output. With a speedup of four, and use of a "most urgent packet first" method of operation, the switch can behave identically to an output-queued switch, regardless of the arriving traffic's nature. The switch therefore performs as if it were output-queued, yet uses memory that runs more slowly.